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**TRANSMITTAL  
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(to be used for all correspondence after initial filing)

Application Number	10/670,567
Filing Date	09/26/2003
First Named Inventor	Herbert Taucher
Art Unit	2133
Examiner Name	to be assigned
Attorney Docket Number	2002P15288US

Total Number of Pages in This Submission

8

**ENCLOSURES (Check all that apply)**

<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to a Technology Center (TC)
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<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s) _____	
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<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	1. Transmittal Form; 2. Copy of the 1. page of the Updated Filing Receipt; 3. Request for Corrected Filing Receipt; 4. Return Post Card; <b>AND</b> <b>5. EXECUTED DECLARATION (COPY).</b>	

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm or Individual	Jacob Eisenberg, Reg. No. 43,410; Customer No. 28,204 Siemens Schweiz AG, Intellectual Property Department, I-44, Albisriederstrasse 245, CH-8047, Zurich, Switzerland
Signature	<i>Jacob Eisenberg</i>
Date	February 26, 2004

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Herbert Taucher *et al.*

Art Unit: 2133

Serial No.: 10/670,567

Examiner: To be assigned

Filing Date: 09/26/2003

Docket No.: 2002P15288US

For: Method and device for testing the mapping/implementation of a model of a logic circuit onto/in a hardware emulator

Assistant Commissioner for Patents  
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**REQUEST FOR CORRECTED UPDATED FILING RECEIPT**

Dear Sir or Madam:

Via DHL, Pages 2

Applicants hereby request that a corrected Updated Filing Receipt be issued in the above-identified patent application. The official Updated Filing Receipt received by Applicants, a copy of which is attached hereto, has the following inaccuracies appearing thereon as indicated by quotation marks and herein requested corrections for which are indicated by double dashes. Please change the Applicants from:

-- Herbert Taucher, Residence Not Provided;  
Karlheinz Krause, Residence Not Provided;  
Majid Ghameshlu, Residence Not Provided;--

to:

"Herbert Taucher, Moedling, Austria;  
Karlheinz Krause, Planegg, Germany; and  
Majid Ghameshlu, Wien, Austria".

Applicants enclose a true copy of the executed declaration for the above application, filed January 12, 2004, evidencing the above addresses.

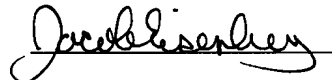
The Patent and Trademark Office is invited to contact the undersigned for any reason which would expedite the handling of this matter. In the event that the Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No.: 502464** referencing docket no.: 2002P15288US. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Date: 02-26-2004

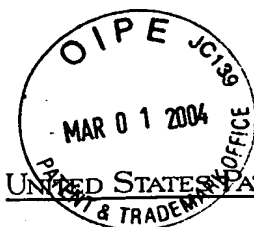
Siemens Schweiz  
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Albisriederstrasse 245  
Zurich, CH-8047 Switzerland

**Enclosures:** Official Filing Receipt (copy),  
Return Card (original), and  
Declaration (copy).

Respectfully submitted,



Jacob Eisenberg  
Attorney for Applicant  
Registration Number 43,410  
**CUSTOMER NUMBER: 28204**



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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/670,567	09/26/2003	2133	880	2002P15288US	2	9	2

CONFIRMATION NO. 2326

## UPDATED FILING RECEIPT



\*OC000000011942994\*

28204  
 SIEMENS SCHWEIZ  
 I-44, INTELLECTUAL PROPERTY  
 ALBISRIEDERSTRASSE 245  
 ZURICH, CH-8047  
 SWITZERLAND

Unterlagen erhalten

25. Feb. 2004

Siemens Schweiz AG

Date Mailed: 02/20/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Herbert Taucher, Residence Not Provided;  
 Kartheinz Krause, Residence Not Provided;  
 Majid Ghameshlu, Residence Not Provided;

## Domestic Priority data as claimed by applicant

## Foreign Applications

EUROPEAN PATENT OFFICE (EPO) 02 021 974.7 09/30/2002

If Required, Foreign Filing License Granted: 12/17/2003

Projected Publication Date: 06/03/2004

Non-Publication Request: No

Early Publication Request: No

## Title

Method and device for testing the mapping/implementation of a model of a logic circuit onto/in a hardware emulator